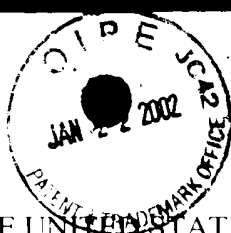


09/045,507



-1-

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Donald Malcolm MacIntyre

Application No.: 09/045,507

Filed: March 20, 1998

For: CHIP SCALE PACKAGES

Group Art Unit: 2814 TC 2800 MAIL ROOM

Examiner: D. Wille

**RESPONSE TO FINAL REJECTION  
MAILED JULY 3, 2001**

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Commissioner for Patents  
Washington, D.C. 20231

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope, addressed to: Commissioner for Patents, Washington, DC 20231 on November 29, 2001.

STALLMAN & POLLOCK LLP

Dated: 11/29/2001

By: Georgia K. Stith

Georgia K. Stith

Sir:

Please amend the above-identified application as follows:

**IN THE CLAIMS**

Please cancel claims 39-48 and add the following new claims:

--49. (New) A semiconductor integrated circuit wafer scale structure comprising:

a semiconductor wafer substrate that includes a plurality of semiconductor integrated circuit die formed on an upper surface of the wafer substrate, each semiconductor integrated circuit die formed on the wafer substrate including a plurality of conductive die bond pads formed on an upper surface of said integrated circuit die;

a unitary, substantially planar glass sheet having substantially the same size as the wafer substrate and having a plurality of prefabricated holes formed therethrough from an inner surface of the glass sheet to a lower surface of the glass sheet, each prefabricated